CLAIMS

1. A semiconductor memory device which has a redundancy circuit comprising:

a plurality of memory blocks; and

a plurality of redundancy memory blocks provided for each of said plurality of memory blocks,

wherein an address bit for selecting each of said plurality of memory blocks is different from an address bit for selecting each of said plurality of redundancy memory blocks.

2. The semiconductor memory device according to claim 1,

wherein one or more adjacent memory cell rows or columns owned by each of said plurality of memory blocks is a segment which is a unit of allocation as a replacement target, and adjacent segments having defects are replaced by different redundancy memory blocks of said plurality of redundancy memory blocks.

3. The semiconductor memory device according to claim 2,

wherein address bits that define said segment are lower address bits, and address bits for selecting said plurality of redundancy memory blocks include an address bit immediately above said lower address bits.

4. The semiconductor memory device according to claim 2,

wherein a unit of said segment is equal to said number of sub word lines.

5. A semiconductor memory device comprising:

a memory block having a plurality of segments, each of said plurality of segments including a plurality of memory cells; and

a plurality of redundancy memory blocks which are provided for said memory block,

wherein each of said plurality of redundancy memory blocks has a redundancy segment which substitutes for any segment having a defect among said plurality of segments,

said plurality of segments are cyclically and sequentially allocated to said plurality of redundancy memory blocks, and

each of said plurality of segments is replaceable by said allocated redundancy memory block when having a defect.

6. A semiconductor memory device comprising:

a plurality of memory blocks each of which has a plurality of segments, each of said plurality of segments including a plurality of memory cells;

and

a plurality of redundancy memory blocks which are provided for said plurality of memory blocks,

wherein each of said plurality of redundancy memory blocks has a redundancy segment which substitutes for any segment having a defect among said plurality of segments,

said plurality of segments are cyclically and sequentially allocated to said plurality of redundancy memory blocks, and

each of said plurality of segments is replaceable by said allocated redundancy memory block when having a defect.

7. A semiconductor memory device having a plurality of memory blocks, wherein each of said plurality of memory blocks includes a plurality of segments,

a redundancy memory block, which substitutes for any segment having a defect of said plurality of segments, is physically provided to each of said plurality of memory blocks,

said redundancy memory block is logically allocated to said plurality of memory blocks in common, and

each of said plurality of segments is replaceable by said allocated redundancy memory block

when having a defect.

8. The semiconductor memory device according to any one of claims 5 to 7,

wherein a first segment and a second segment of said plurality of segments are adjacent to each other, and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks.

9. The semiconductor memory device according to claim 8,

wherein an address indicating said first segment and an address indicating said second segment are successive addresses, and a number indicating said first redundancy memory block and a number indicating said second redundancy memory block are cyclically successive.

10. The semiconductor memory device according to any one of claims 5 to 9,

wherein a number indicating said redundancy memory block allocated to any of said plurality of segments is given by a remainder generated when an address indicating said any segment is divided by a number of said redundancy memory blocks.

11. The semiconductor memory device according to any one of claims 5 to 10,

wherein each of said plurality of segments is a group of memory cells connected to 2^n (n=0, 1, 2,...) word lines or bit lines, and when a number of said word lines or said bit lines is plural, said word lines or said bit lines are adjacent.

12. The semiconductor memory device according to any one of claims 5 to 11,

wherein a plurality of lower bits of an address inputted to a decode circuit for selecting any of said plurality of segments are inputted to a decode circuit for selecting said redundancy memory blocks.